

Electric-field control of spin accumulation signals in silicon at room temperature

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We demonstrate spin-accumulation signals controlled by the gate voltage in a metal-oxide-semiconductor field effect transistor structure with a Si channel and a CoFe/ n^+ -Si contact at room temperature. Under the application of a back-gate voltage, we clearly observe the three-terminal Hanle-effect signal, i.e., spin-accumulation signal. The magnitude of the spin-accumulation signals can be reduced with increasing the gate voltage. We consider that the gate controlled spin signals are attributed to the change in the carrier density in the Si channel beneath the CoFe/ n^+ -Si contact. This study is not only a technological jump for Si-based spintronic applications with gate structures but also reliable evidence for the spin injection into the semiconducting Si channel at room temperature.

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The progress of silicon-based spintronics (Si spintronics) is splendid in recent years. Many groups have so far demonstrated electrical spin injection and detection through ferromagnet-insulator-Si heterostructures.[1–6] Recently, spin-related phenomena at room temperature were reported in Si-based three- or four-terminal lateral devices.[4–6] In particular, clear room-temperature spin transport and its manipulation by applying transverse magnetic fields were achieved although the channel used was a heavily doped Si.[5]

To date, we have explored the spin injection and detection in Si-based devices without insulators for source and drain contacts in order to reduce the parasitic resistance.[7, 8] Recently, we studied spin accumulation signals at a ferromagnetic CoFe/ n^+ -Si interface by measuring a Hanle effect in three-terminal lateral devices,[8] and found that there is an electrical detectability of the contact for spin accumulation in the Si channel, consistent with the previous work in Fe/GaAs lateral devices.[11] If the Hanle-effect signals are arising from the spin accumulation in the Si channel, we should observe the variation in the Hanle-effect signals by changing carrier densities in the Si channel.[6, 11]

In this letter, we demonstrate spin-accumulation signals controlled by the gate voltage in a Si-metal-oxide-semiconductor field effect transistor (MOSFET) structure with a CoFe/ n^+ -Si contact at room temperature. Under the application of a back-gate voltage, we clearly observe the three-terminal Hanle-effect signal, i.e., spin-accumulation signal. The magnitude of the spin-accumulation signals can be reduced with increasing the gate voltage. We consider that the gate controlled spin

signals can be explained by the change in the carrier density in the Si channel beneath the CoFe/ n^+ -Si contact. This is reliable evidence for the spin injection into the semiconducting Si channel at room temperature. From the technological point of view, this study will lead to an acceleration of research and development of Si-based spintronic applications with gate structures.[9, 10]

Ferromagnetic CoFe epitaxial layers with a thickness of ~ 10 nm were grown on (111)-oriented Silicon On Insulator (SOI) by low-temperature molecular beam epitaxy (MBE) at $\sim 25^\circ\text{C}$, [12] where the thicknesses of the SOI and buried oxide (BOX) layers are about ~ 75 and 200 nm, respectively, and the carrier density of the SOI layer is $\sim 4.5 \times 10^{15}\text{cm}^{-3}$ ($1 \sim 5 \Omega\text{cm}$) at room temperature. By a combination of the Si epitaxy using an MBE process with an Sb δ -doping technique, an n^+ -Si layer (Sb : $1 \times 10^{19}\text{cm}^{-3}$) was inserted between CoFe and SOI. Here the Sb δ -doped n^+ -Si layer on the channel region was removed by the Ar^+ ion milling. An ohmic contact (AuSb) for backside heavily doped Si was formed at less than 300°C . Conventional processes with electron-beam lithography, Ar^+ ion milling, and reactive ion etching were used to fabricate three-terminal lateral devices with a backside gate electrode, illustrated in Fig. 1(a). The CoFe/ n^+ -Si contact (contact 2) and AuSb ohmic contacts (contact 1 and 3) have lateral dimensions of $1 \times 100 \mu\text{m}^2$ and $100 \times 100 \mu\text{m}^2$, respectively. The distance between the contacts 2 and 1 or 3 is $\sim 30 \mu\text{m}$. The three-terminal Hanle measurements were performed by a dc method with the current-voltage configuration shown in Fig. 1(a) at room temperature, where a small magnetic field perpendicular to the plane, B_z , was applied after the magnetic moment of the contact 2 aligned parallel to the plane along the long axis of the contact.

First, we confirm the operation as a MOSFET for the fabricated device shown in Fig. 1(a). Figure 1(b) shows

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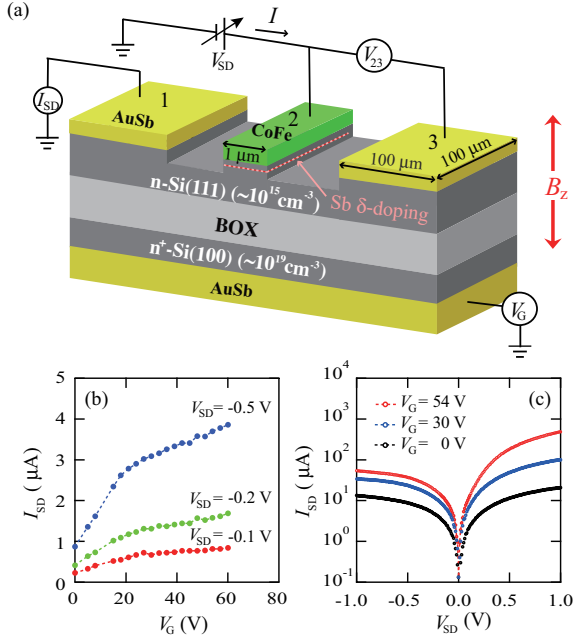


FIG. 1: (Color online) (a) Schematic diagram of a Si-MOSFET structure with a CoFe/ n^+ -Si Schottky-tunnel contact fabricated. (b) $I_{SD}-V_G$ and (c) $I_{SD}-V_{SD}$ characteristics at room temperature. The constant V_{SD} and V_G values are denoted in each figure.

$I_{SD}-V_G$ characteristic measured at room temperature at constant bias voltages of $V_{SD} = -0.1, -0.2$, and -0.5 V. With increasing V_G , the I_{SD} value gradually increases for all V_{SD} . This means that the conduction channel is formed from the vicinity of the interface between SOI and BOX. These results clearly indicate that this device can operate as a MOSFET. Because of relatively thick SOI layer, the carrier density of the bulk SOI is still enhanced by further applying V_G . Hence, the I_{SD} value is not saturated in high V_G region. Figure 1(c) displays representative $I_{SD}-V_{SD}$ characteristics at room temperature at various V_G . Almost symmetric and nonlinear characteristics were observed up to $V_G = 20$ V but small asymmetric features with respect to the bias polarity can be seen in $V_G > 20$ V. Since these features are markedly different from those resulting from the thermionic emission examined previously in Ref.[12], tunneling conduction through the CoFe/ n^+ -Si interface is dominant factor for the observed $I_{SD}-V_{SD}$ characteristics at room temperature. Although we could not make the evident off state at $V_G = 0$ V for this device, as shown in Fig. 1(b), there is almost no influence on the main claim of this study.

Using this device, we measured the three-terminal voltage, ΔV_{23} , as a function of B_Z , i.e., Hanle effect. Figure 2(a) shows a $\Delta V_{23}-B_Z$ curve for $V_G = 8.0$ V at $I_{SD} = -1.0$ μ A at room temperature, where a quadratic background voltage depending on B_Z is subtracted from the raw data. Here in this condition ($I_{SD} < 0$) the electrons are injected from the spin-polarized states of CoFe into

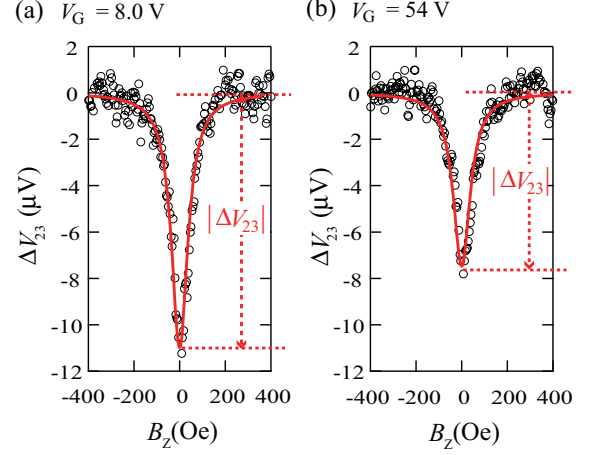


FIG. 2: (Color online) Room-temperature spin accumulation signals measured at (a) $V_G = 8.0$ V and (b) $V_G = 54$ V. The applied bias current is a constant value of $I_{SD} = -1.0$ μ A, which induces spin accumulation in a Si conduction band by spin injection from CoFe into Si. The red curves are fitting results by the Lorentzian function.

the conduction band of Si. When B_Z increases from zero to ± 200 Oe, a clear voltage change ($|\Delta V_{23}|$) is observed even at room temperature. The voltage change is caused by the depolarization of the accumulated spins, that is, a Hanle-type spin precession is detected by the three-terminal voltage measurements.[4, 6, 8, 11, 13, 14] We could not obtain such Hanle-effect curves in $V_G < 8.0$ V because the electrical noise was very large. We hereafter concentrate on a constant injection current of $I_{SD} = -1.0$ μ A for examining the effect of the application of V_G ($V_G \geq 8.0$ V) though the Hanle-effect signals can easily be enhanced by increasing the injection current.[8] We note that the magnitude of ΔV_{23} , $|\Delta V_{23}|$, is ~ 11.5 μ V in Fig. 2(a). Surprisingly, $|\Delta V_{23}|$ is decreased to ~ 7.8 μ V when the gate voltage is further applied up to $V_G = 54$ V in Fig. 2(b). For both V_G conditions, a lower limit of spin lifetime (τ_S) can be obtained using the Lorentzian function, $\Delta V_{23}(B_Z) = \Delta V_{23}(0)/[1+(\omega_L \tau_S)^2]$, where $\omega_L = g\mu_B B_Z/\hbar$ is the Larmor frequency, g is the electron g -factor ($g = 2$), μ_B is the Bohr magneton.[4] The fitting results are denoted by the red solid curves in Fig. 2. The τ_S values for $V_G = 8.0$ and 54 V are estimated to be ~ 1.30 and ~ 1.27 nsec, respectively. It seems that the τ_S value is almost constant despite the change in $|\Delta V_{23}|$.

On the basis of the simple spin diffusion model,[15–18] we consider the observed $|\Delta V_{23}|$. For three-terminal measurements, the magnitude of the voltage change due to the Hanle-type spin precession can be expressed as follows:[14]

$$\frac{\Delta V}{I} = \frac{P^2 \lambda_N \rho_N}{2A}, \quad (1)$$

where P is the spin polarization, λ_N and ρ_N are the spin diffusion length and resistivity of the nonmagnet

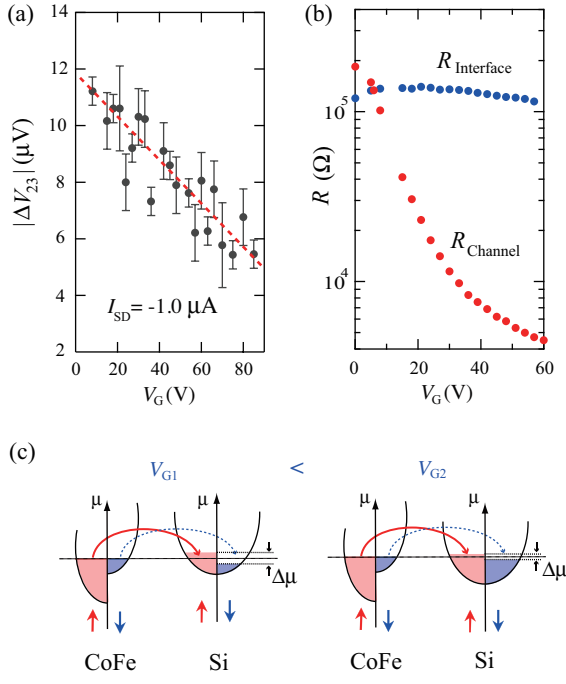


FIG. 3: (Color online) (a) $|\Delta V_{23}|$ as a function of V_G for $I_{SD} = -1.0 \mu A$ at room temperature. (b) The changes in $R_{Channel}$ and $R_{Interface}$ with increasing V_G at room temperature. (c) Schematic diagrams of the change in the spin accumulation ($\Delta\mu$) by the application of V_G .

used, respectively. A is the contact area. For our fabricated device, when we assume $D \sim 40 \text{ cm}^2\text{s}^{-1}$ ($n \sim 10^{15}\text{cm}^{-3}$), [19] $\lambda_{Si} \sim 2.3 \mu\text{m}$ is obtained by using the relationship of $\lambda_N = \sqrt{D\tau_S}$ ($\tau_S \sim 1.3 \text{ nsec}$). Also, $\rho_{Si} = 1 \sim 5 \Omega\text{cm}$ at room temperature is assumed. Since the spin resistance-area-product (spin- RA), $\frac{\Delta V_{23}}{I_{SD}} \times A$, is obtained to be $\sim 1.15 \text{ k}\Omega\mu\text{m}^2$ for the data in Fig. 2(a), we can roughly obtain $0.14 < P < 0.32$ using Eq.(1). The obtained P is consistent with that for CoFe alloys expected.[20] Therefore, our Hanle-effect signals observed here can roughly be considered within the framework of the commonly used diffusion model.[15–18]

To discuss the origin of the reduction in $|\Delta V_{23}|$ in Fig. 2, we explored Hanle-effect signals for various V_G in detail. Figure 3(a) displays $|\Delta V_{23}|$ vs V_G at $I_{SD} = -1.0 \mu A$ at room temperature. With increasing V_G , nearly linear decrease in $|\Delta V_{23}|$ is obtained. Thus, the observed feature in Fig. 2 is reproduced systematically. Here we also examine the V_G dependence of channel resistance ($R_{Channel}$) and interface resistance ($R_{Interface}$) at room temperature, where $R_{Channel}$ and $R_{Interface}$ can roughly be obtained by using local and nonlocal three-terminal measurements, respectively. As shown in Fig. 3(b), $R_{Channel}$ decreases with increasing V_G while $R_{Interface}$ is almost constant irrespective of V_G . [21] Here we focus on the change in $R_{Channel}$ by the application of V_G . Since

the thickness of SOI layer is relatively thick ($\sim 75 \text{ nm}$), all the changed $R_{Channel}$ values after the application of V_G are not directly associated with the change in ρ_{Si} of all the channel regions in this device. However, the application of V_G should affect the partial change in ρ_{Si} of the Si channel at least because $R_{Channel}$ does not saturate with increasing V_G . Thus, the carrier density in the Si channel beneath the CoFe/ n^+ -Si contact should be enhanced by applying V_G . From these considerations, the monotonous decrease in $|\Delta V_{23}|$ with applying V_G can be explained by the decrease in ρ_N in Eq. (1), where ρ_N is ρ_{Si} of the Si channel beneath the CoFe/ n^+ -Si contact.

Phenomenological schematic diagrams of the spin accumulation in the Si channel beneath the CoFe/ n^+ -Si contact are shown in Fig. 3(c). Under a condition for spin injection into Si, the spin accumulation ($\Delta\mu$) occurs in the Si conduction band near the quasi Fermi level (left figure). When we increase V_G from V_{G1} to V_{G2} , the carrier density in the Si conduction channel beneath the CoFe/ n^+ -Si contact increases, causing the decrease in ρ_{Si} . Namely, even if the same I_{SD} is used for spin injection into the Si channel, tunneling probability of spin-polarized electrons and the density of state in Si at the Fermi level should be varied by the application of V_G , resulting in the reduction in $\Delta\mu$ (right figure). Accordingly, the experimental data can also be explained within a framework based on the simple diffusion model [Eq.(1)]. We note that the present study including gate-induced change in the Hanle-effect signals is exact evidence for the detection of spin-polarized electrons created not in the localized state in the vicinity of the interface but in the Si channel. We convince that the three-terminal Hanle-effect measurements are powerful tool for detection of the spin accumulation in the semiconductor channels.

In summary, we have demonstrated electric-field control of spin accumulation in Si using a MOSFET structure with a CoFe/ n^+ -Si contact. Even at room temperature, we observed clear spin accumulation signals under an application of the gate voltage. The magnitude of the spin accumulation signals was reduced by the increase in the gate voltage. We consider that the reduction in the spin-accumulation signals is attributed to the increase in the carrier density in the Si channel beneath the CoFe/ n^+ -Si contact, indicating reliable evidence for the spin injection into the semiconducting Si channel at room temperature. This study also includes a technological jump for Si-based spintronic applications with gate structures.

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- [1] I. Appelbaum, B. Huang, and D. J. Monsma, *Nature* **447**, 295 (2007); B. Huang, D. J. Monsma, and I. Appelbaum, *Phys. Rev. Lett.* **99**, 177209 (2007); H.-J. Jang and I. Appelbaum, *Phys. Rev. Lett.* **103**, 117202 (2009); Y. Lu, J. Li, and I. Appelbaum, *Phys. Rev. Lett.* **106**, 217202 (2011).
 - [2] B. T. Jonker, G. Kioussoglou, A. T. Hanbicki, C. H. Li, and P. E. Thompson, *Nat. Phys.* **3**, 542 (2007); O. M. J. van't Erve, A. T. Hanbicki, M. Holub, C. H. Li, C. Awo-Affouda, P. E. Thompson, and B. T. Jonker, *Appl. Phys. Lett.* **91**, 212109 (2007).
 - [3] T. Sasaki, T. Oikawa, T. Suzuki, M. Shiraishi, Y. Suzuki, and K. Tagami, *Appl. Phys. Express* **2**, 053003 (2009); T. Sasaki, T. Oikawa, T. Suzuki, M. Shiraishi, Y. Suzuki, and K. Noguchi, *IEEE Trans. Mag.* **46**, 1436 (2010); M. Shiraishi, Y. Honda, E. Shikoh, Y. Suzuki, T. Shinjo, T. Sasaki, T. Oikawa, K. Noguchi, and T. Suzuki, *Phys. Rev. B* **83**, 241204(R) (2011).
 - [4] S. P. Dash, S. Sharma, R. S. Patel, M. P. Jong, and R. Jansen, *Nature (London)* **462**, 491 (2009); R. Jansen, B. C. Min, S. P. Dash, S. Sharma, G. Kioussoglou, A. T. Hanbicki, O. M. J. van't Erve, P. E. Thompson, and B. T. Jonker, *Phys. Rev. B* **82**, 241305(R) (2010).
 - [5] T. Suzuki, T. Sasaki, T. Oikawa, M. Shiraishi, Y. Suzuki, and K. Noguchi, *Appl. Phys. Express* **4**, 023003 (2011).
 - [6] C. H. Li, O. M. J. van't Erve, and B. T. Jonker, *Nat. Commun.* **2**, 245 (2011).
 - [7] Y. Ando, K. Hamaya, K. Kasahara, Y. Kishi, K. Ueda, K. Sawano, T. Sadoh, and M. Miyao, *Appl. Phys. Lett.* **94**, 182105 (2009); Y. Ando, K. Kasahara, K. Yamane, K. Hamaya, K. Sawano, T. Kimura, and M. Miyao, *Appl. Phys. Express* **3**, 093001 (2010).
 - [8] Y. Ando, K. Kasahara, K. Yamane, Y. Baba, Y. Maeda, Y. Hoshi, K. Sawano, M. Miyao, and K. Hamaya, *Appl. Phys. Lett.* **98**, 262102 (2011).
 - [9] S. Sugahara and M. Tanaka, *Appl. Phys. Lett.* **84**, 2307 (2004).
 - [10] H. Dery, P. Dalal, L. Cywiński, and L. J. Sham, *Nature (London)* **447**, 573 (2007).
 - [11] X. Lou, C. Adelman, M. Furis, S. A. Crooker, C. J. Palmström, and P. A. Crowell, *Phys. Rev. Lett.* **96**, 176603 (2006); S. A. Crooker, E. S. Garlid, A. N. Chantis, D. L. Smith, K. S. M. Reddy, Q. O. Hu, T. Kondo, C. J. Palmström, and P. A. Crowell, *Phys. Rev. B* **80**, 041305(R) (2009); M. K. Chan, Q. O. Hu, J. Zhang, T. Kondo, C. J. Palmström, and P. A. Crowell, *Phys. Rev. B* **80**, 161206(R) (2009).
 - [12] Y. Maeda, K. Hamaya, S. Yamada, Y. Ando, K. Yamane, and M. Miyao, *Appl. Phys. Lett.* **97**, 192501 (2010).
 - [13] M. Tran, H. Jaffrès, C. Deranlot, J. -M. George, A. Fert, A. Miard, and A. Lemaître, *Phys. Rev. Lett.* **102**, 036601 (2009).
 - [14] T. Sasaki, T. Oikawa, M. Shiraishi, Y. Suzuki, and K. Noguchi, *Appl. Phys. Lett.* **98**, 012508 (2011).
 - [15] A. Fert and H. Jaffrès, *Phys. Rev. B* **64**, 184420 (2001).
 - [16] F. J. Jedema, H. B. Heersche, A. T. Filip, J. J. A. Baselmans, and B. J. van Wees, *Nature* **416**, 713 (2002).
 - [17] S. Takahashi and S. Maekawa, *Phys. Rev. B* **67**, 052406 (2003).
 - [18] H. Dery, L. Cywiński, and L. J. Sham, *Phys. Rev. B* **73**, 041306(R) (2006).
 - [19] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York 1981), pp. 27-30.
 - [20] For example, D. J. Monsma and S. S. P. Parkin, *Appl. Phys. Lett.* **77**, 720 (2000).
 - [21] From this data, we can estimate the tunnel resistance of the CoFe/ n^+ -Si interface, $R_{\text{Interface}} \times A$, to be $\sim 10^7 \Omega \mu\text{m}^2$.